



Digital Logic Design
(CS302)
Assignment # 03
Fall 2020

Total marks = 20

Deadline
8 February 2021

Please carefully read the following instructions before attempting the assignment.

RULES FOR MARKING

It should be clear that your assignment would not get any credit if:

- The assignment is submitted after the due date.
- The submitted assignment does not open or the file is corrupt.
- Strict action will be taken if the submitted solution is copied from any other student or the internet.

You should concern the recommended books to clarify your concepts as handouts are not sufficient.

You are supposed to submit your assignment in **Doc or Docx** format.

Any other formats like Scan Images, Pdf, Zip, Rar, Ppt and Bmp, etc will not be accepted.

Topic Covered:

- PAL
- PLA
- GAL
- ABEL

NOTE

No assignment will be accepted **after the due date via email in any case** (whether it is the case of load shedding or internet malfunctioning etc.). Hence refrain from uploading assignments in the last hour of the deadline. It is recommended to upload the solution file at least two days before its closing date.

If you people find any mistake or confusion in the assignment (Question statement), please consult with your instructor before the deadline. After the deadline, no queries will be entertained in this regard.

For any query, feel free to email at:
cs302@vu.edu.pk

Questions No 01

Marks (20)

You are provided with two figures. Figure 1 is a 10 x 5 Programmable Array Logic (PAL) circuit whereas Figure 2 is a 5 x 3 Programmable Logic Array (PLA) circuit. You are required to write An ABEL code/expression for both circuits.

PAL: 10 Inputs (I1, I2, I3, I4, I5, I6, I7, I8, I9, I10) & 5 Outputs (O1, O2, O3, O4, O5).

PLA: 5 Inputs (O1, O2, O3, O4, O5) & 3 Outputs (X, Y, Z).

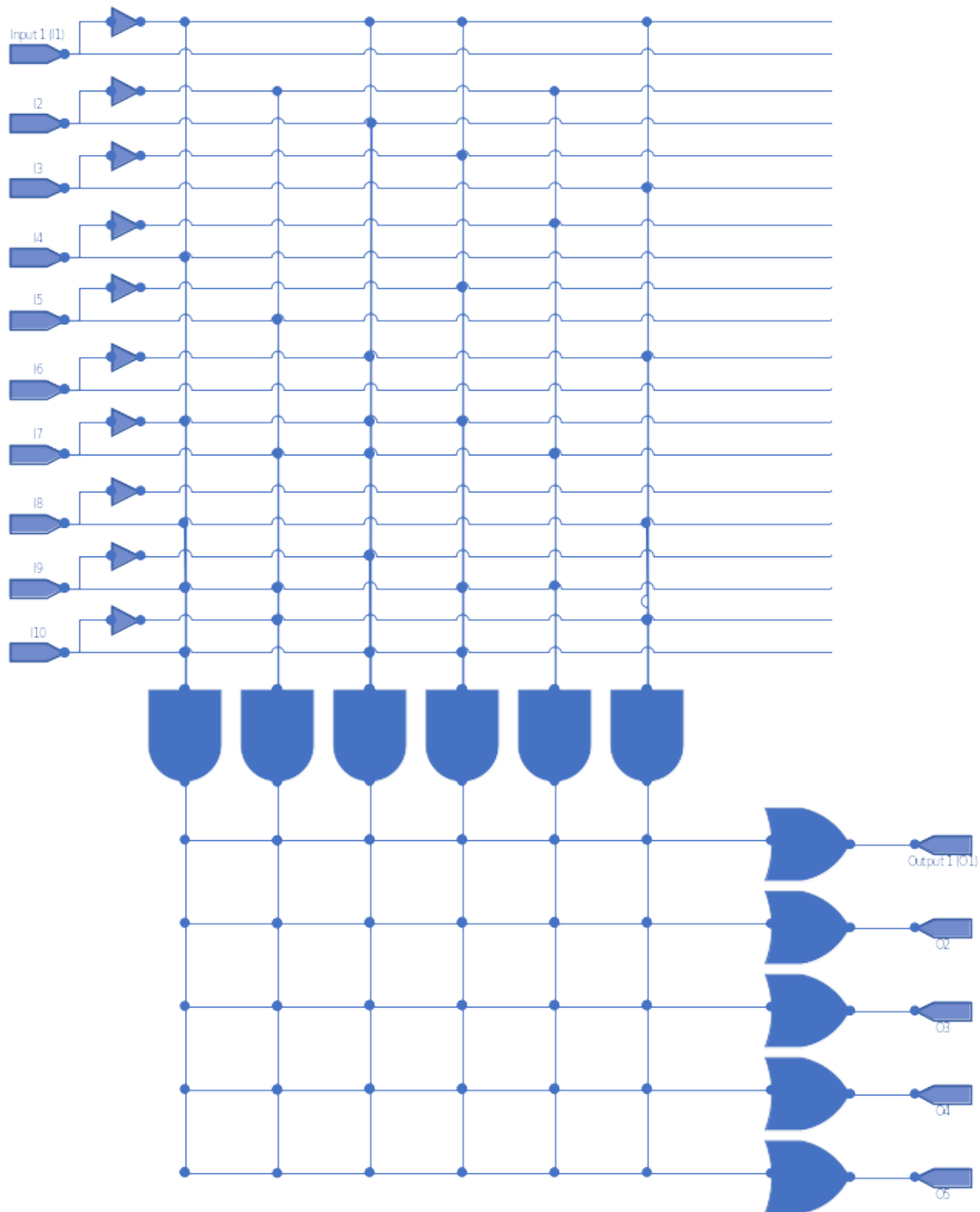


Figure 1: Programmable Array Logic (PAL)

$$P1 = \overline{I1}.I4.\overline{I7}.I8.I9.I10$$

$$P2 = \overline{I2}.I5.I7.I9.\overline{I10}$$

$$P3 = \overline{I1}.I2.\overline{I6}.\overline{I7}.I7.\overline{I9}.I10$$

$$P4 = \overline{I1}.\overline{I3}.\overline{I5}.\overline{I7}.I9.I10$$

$$P5 = \overline{I2}.\overline{I4}.I7.I9$$

$$P6 = \overline{I1}.I3.\overline{I6}.I8.\overline{I10}$$

Sum of terms (SOP)

O1 =

$$\overline{I1}.I4.\overline{I7}.I8.I9.I10+\overline{I2}.I5.I7.I9.\overline{I10}+\overline{I1}.I2.\overline{I6}.\overline{I7}.I7.\overline{I9}.I10+\overline{I1}.I3.\overline{I6}.I8.\overline{I10}$$

O2 =

$$\overline{I1}.I4.\overline{I7}.I8.I9.I10+\overline{I2}.I5.I7.I9.\overline{I10}+\overline{I1}.I2.\overline{I6}.\overline{I7}.I7.\overline{I9}.I10+\overline{I1}.I3.\overline{I6}.I8.\overline{I10}$$

O3 =

$$\overline{I1}.I4.\overline{I7}.I8.I9.I10+\overline{I2}.I5.I7.I9.\overline{I10}+\overline{I1}.I2.\overline{I6}.\overline{I7}.I7.\overline{I9}.I10+\overline{I1}.I3.\overline{I6}.I8.\overline{I10}$$

O4 =

$$\overline{I1}.I4.\overline{I7}.I8.I9.I10+\overline{I2}.I5.I7.I9.\overline{I10}+\overline{I1}.I2.\overline{I6}.\overline{I7}.I7.\overline{I9}.I10+\overline{I1}.I3.\overline{I6}.I8.\overline{I10}$$

O5 =

$$\overline{I1}.I4.\overline{I7}.I8.I9.I10+\overline{I2}.I5.I7.I9.\overline{I10}+\overline{I1}.I2.\overline{I6}.\overline{I7}.I7.\overline{I9}.I10+\overline{I1}.I3.\overline{I6}.I8.\overline{I10}$$

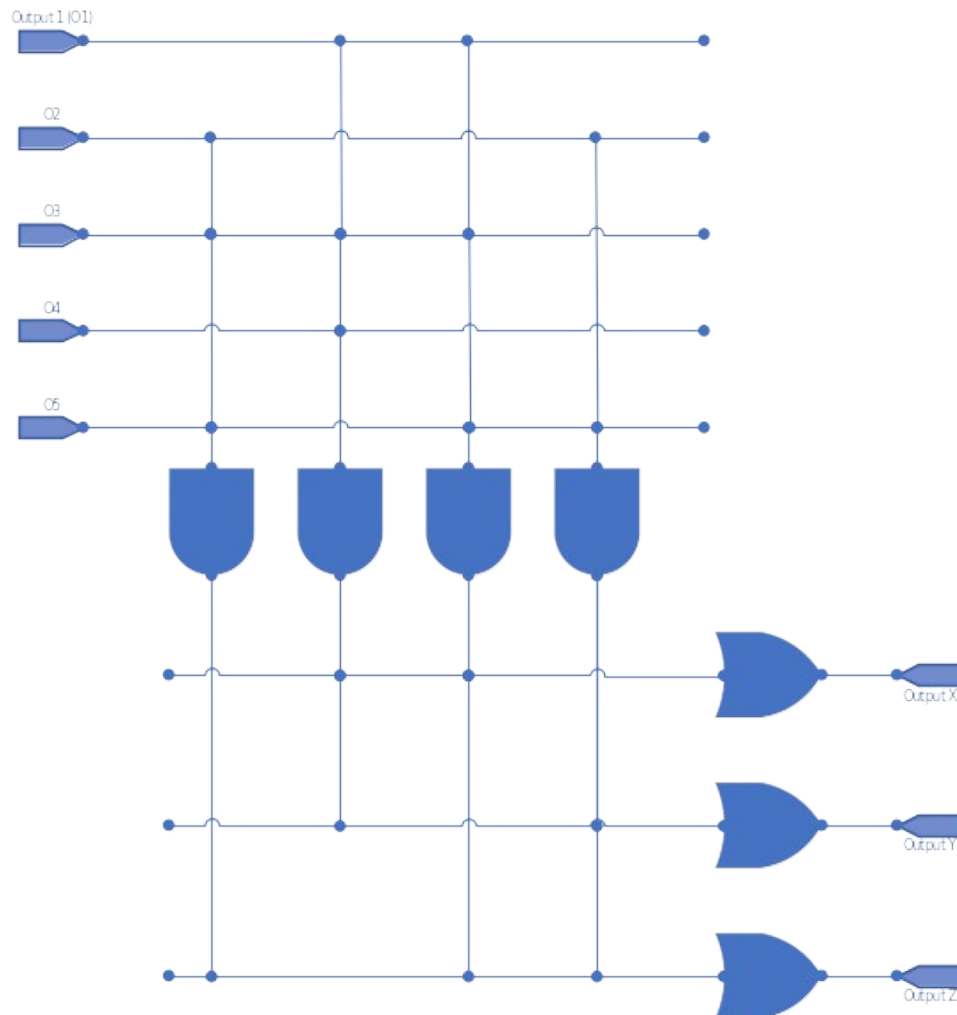


Figure 2: Programmable Logic Array (PLA)