

Digital Logic Design Counters and Registers

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Counters and Registers

- **Counters**

- Asynchronous Counters
- Synchronous Counters
- Design of Synchronous Counters

- **Registers**

- Shift Registers
 - SISO, SIPO, PISO, PIPO

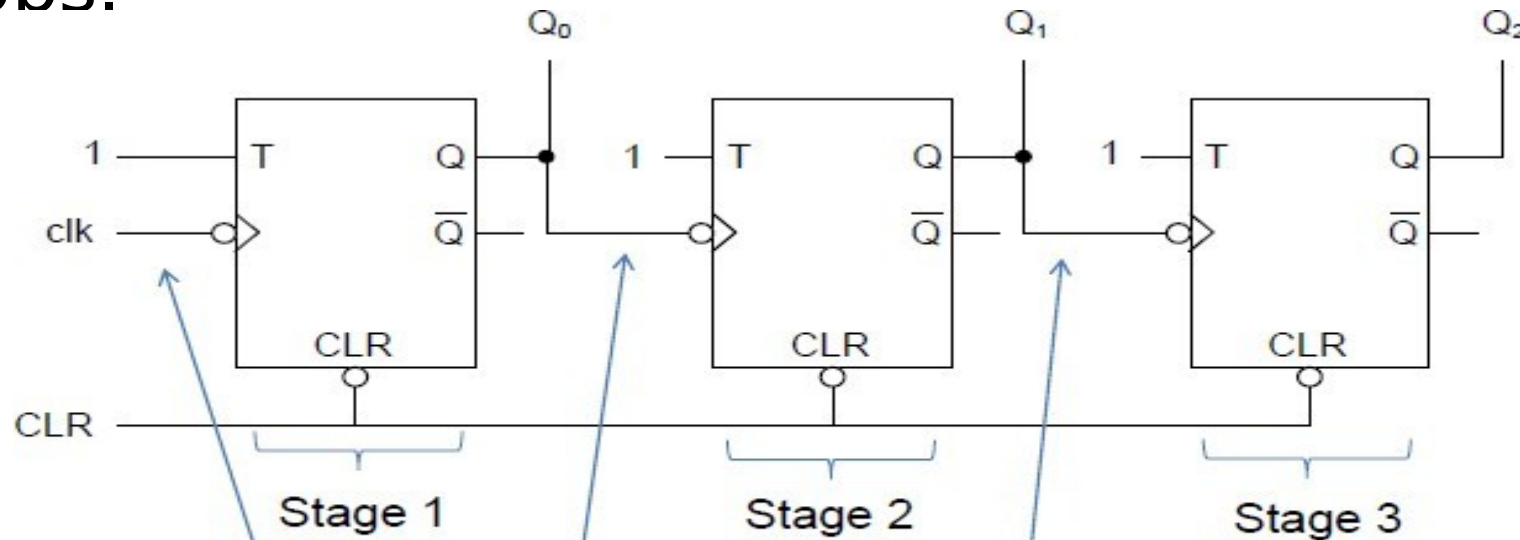
Counte

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- Counters – Circuits that performs the operation of counting at every clock edge.
- Counter are designed using flip-flops, typically the negative edge triggered.
- Counters can be designed as asynchronous or synchronous.
- **Asynchronous counters** – The clock is applied on the first stage. Subsequent stages derive the clock from the pervious stage.
- **Synchronous counters** – The clock is applied to all stages using a common clock signal

Counters – Asynchronous Counters

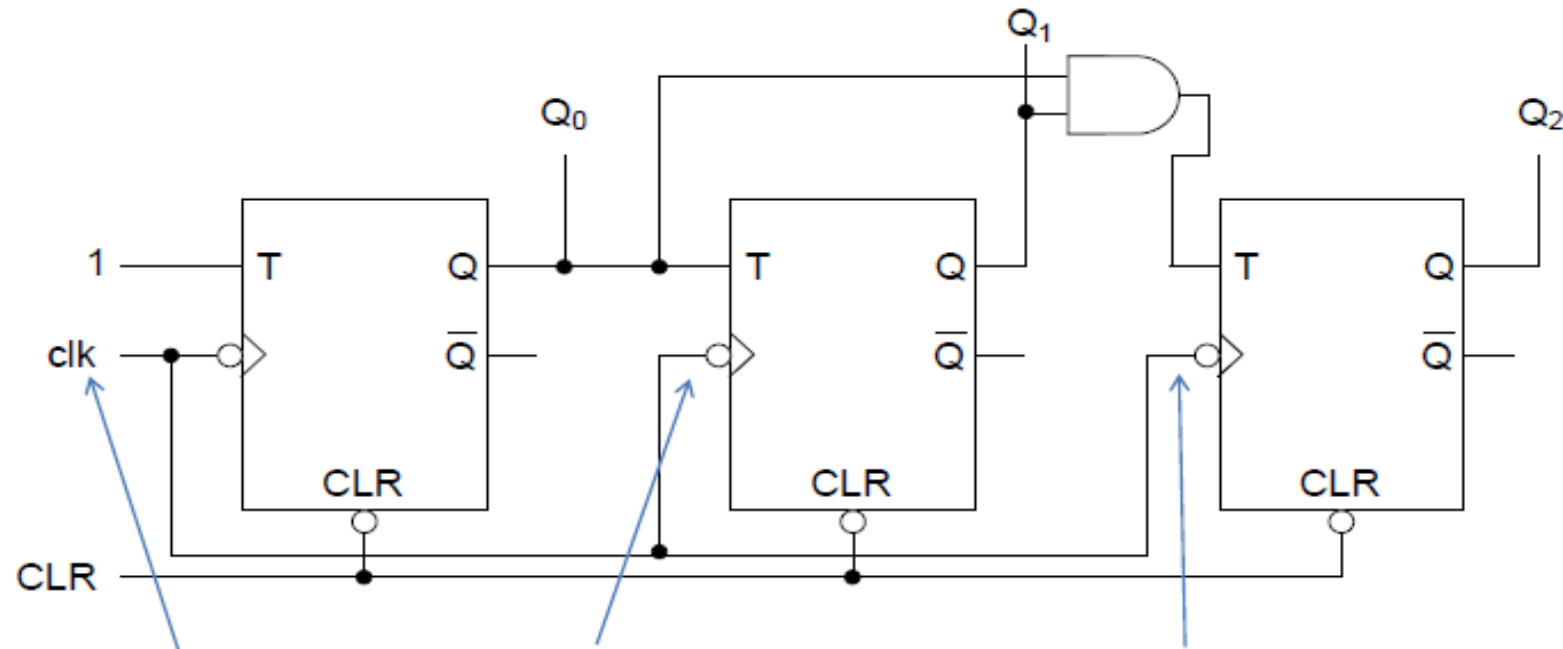
- 3-bit Asynchronous counter using T flip-flops.



In asynchronous counters, the clk signal is fed to the 1st stage only. Subsequent stages take the Q from the previous stage for clk

Counters – Synchronous Counters

- 3-bit Synchronous Counter using T flip-flo



In synchronous counters, a common clk signal is used to clock all flip-flops

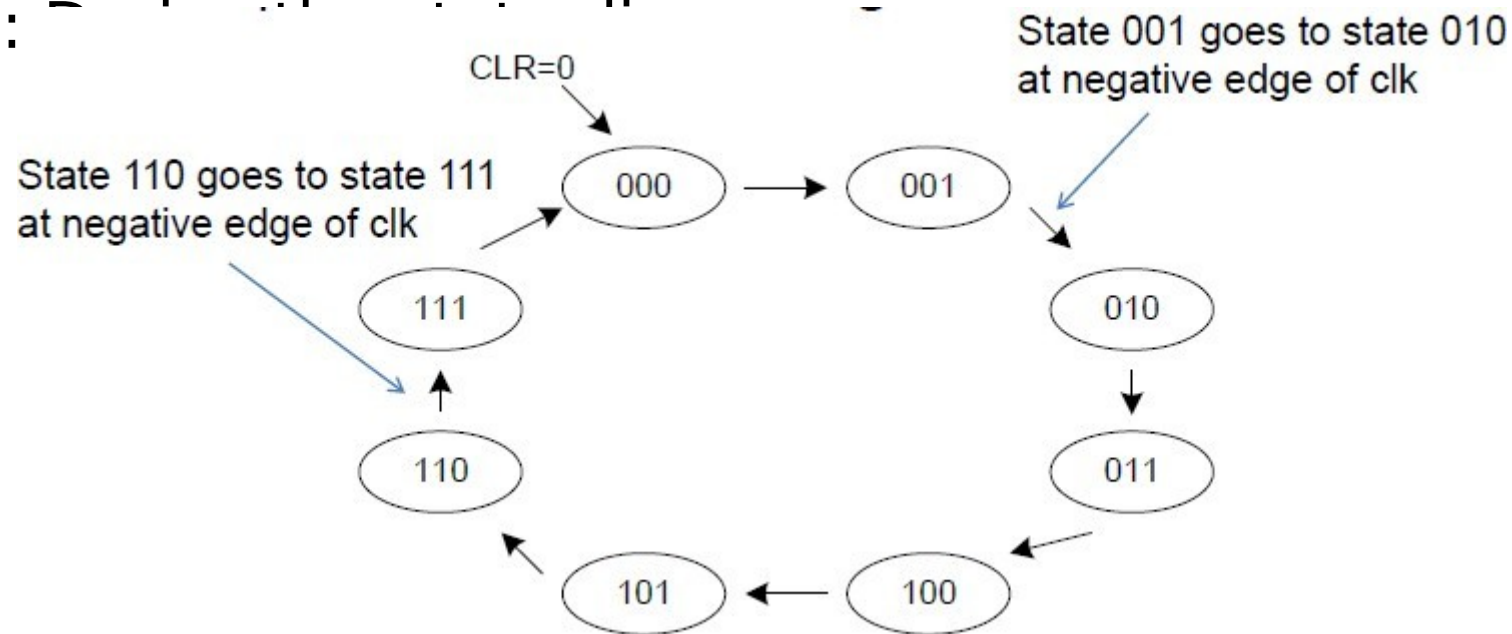
Design of Synchronous Counters

- How to design the 3-bit synchronous counter?
- There are a systematic procedure of designing synchronous counters.
 - Step 1: Derive the state transition diagram
 - Step 2: Derive the next state and state transition table
 - Step 3: Using K-Maps, derive the logic expressions
 - Step 4: Implement the circuit

Design of Synchronous Counters

- The design of triggered 3-bit negative edge synchronous counter using T flip-flops.

• STEP 1:



Design of Synchronous Counters

- Step 2: Derive the next state and state transition table

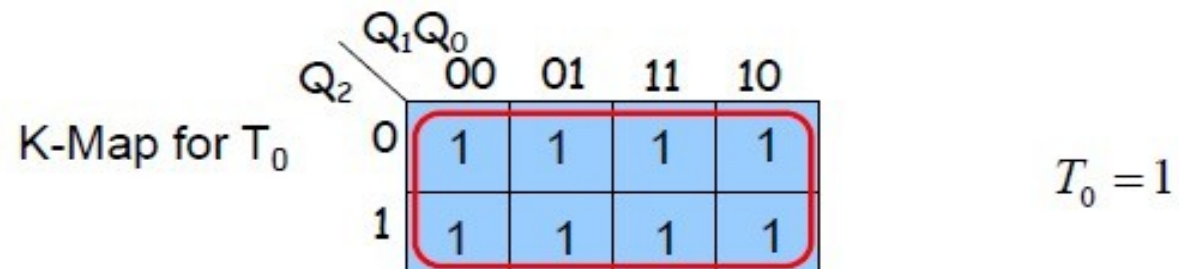
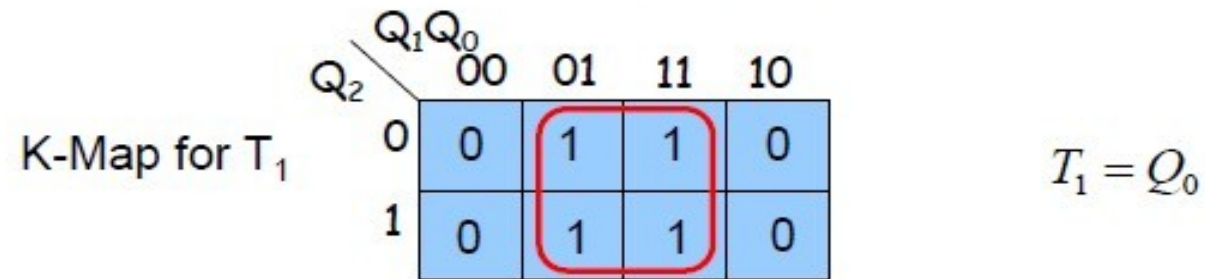
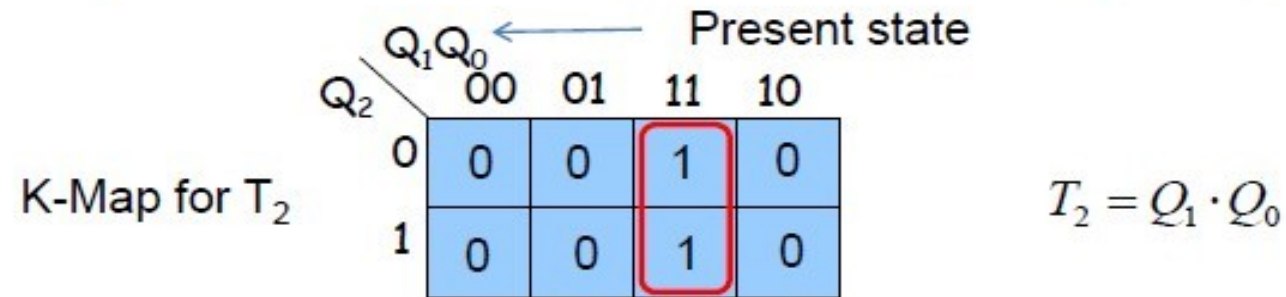
3-bit counter, we need 3 flip-flops

Using T flip-flops

Present State			Next State			Output Transition			Flip-flop Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	T_2	T_1	T_0
0	0	0	0	0	1	$0 \rightarrow 0$	$0 \rightarrow 0$	$0 \rightarrow 1$	0	0	1
0	0	1	0	1	0	$0 \rightarrow 0$	$0 \rightarrow 1$	$1 \rightarrow 0$	0	1	1
0	1	0	0	1	1	$0 \rightarrow 0$	$1 \rightarrow 1$	$0 \rightarrow 1$	0	0	1
0	1	1	1	0	0	$0 \rightarrow 1$	$1 \rightarrow 0$	$1 \rightarrow 0$	1	1	1
1	0	0	1	0	1	$1 \rightarrow 1$	$0 \rightarrow 0$	$0 \rightarrow 1$	0	0	1
1	0	1	1	1	0	$1 \rightarrow 1$	$0 \rightarrow 1$	$1 \rightarrow 0$	0	1	1
1	1	0	1	1	1	$1 \rightarrow 1$	$1 \rightarrow 1$	$0 \rightarrow 1$	0	0	1
1	1	1	0	0	0	$1 \rightarrow 0$	$1 \rightarrow 0$	$1 \rightarrow 0$	1	1	1

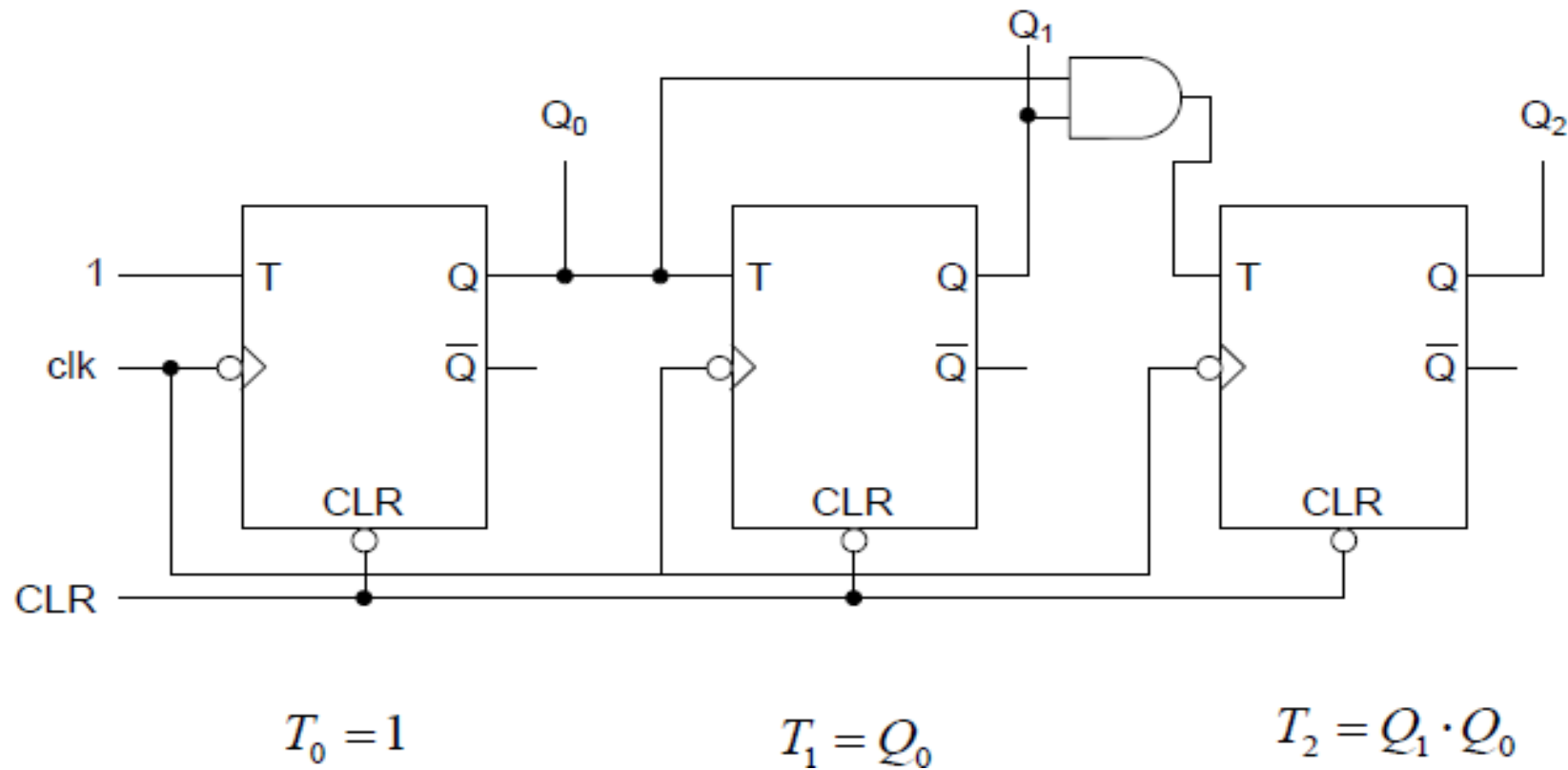
Design of Synchronous

- Step 3: Using K-Maps, derive the logic expressions



Design of Synchronous

- Step 4: Implement the circuit



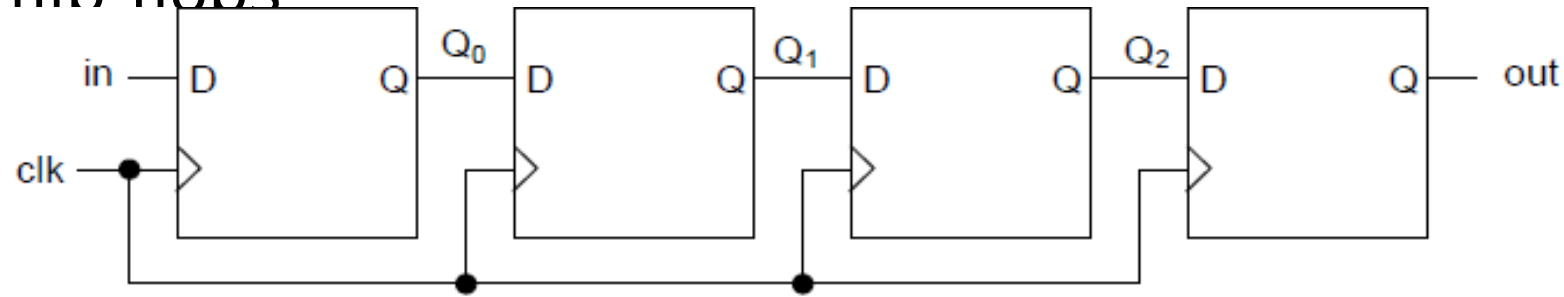
Register – Shift Registers

- Shift registers are used primarily for storage and data movement.
- There are four types of shift registers.
 - Serial In Serial Out – SISO
 - Serial In Parallel Out – SIPO
 - Parallel In Serial Out – PISO
 - Parallel In Parallel Out – PIPO
- All the first registers are arrays of flip-flops, arranged in certain ways.

Serial In Serial Out

- SISO

- 4-bit SISO shift register
 - Each clock pulse will move an input bit to the next flip-flops



when $\text{clk} = \uparrow$

$Q_0 \leftarrow \text{in},$

$Q_1 \leftarrow Q_0$

$Q_2 \leftarrow Q_1$

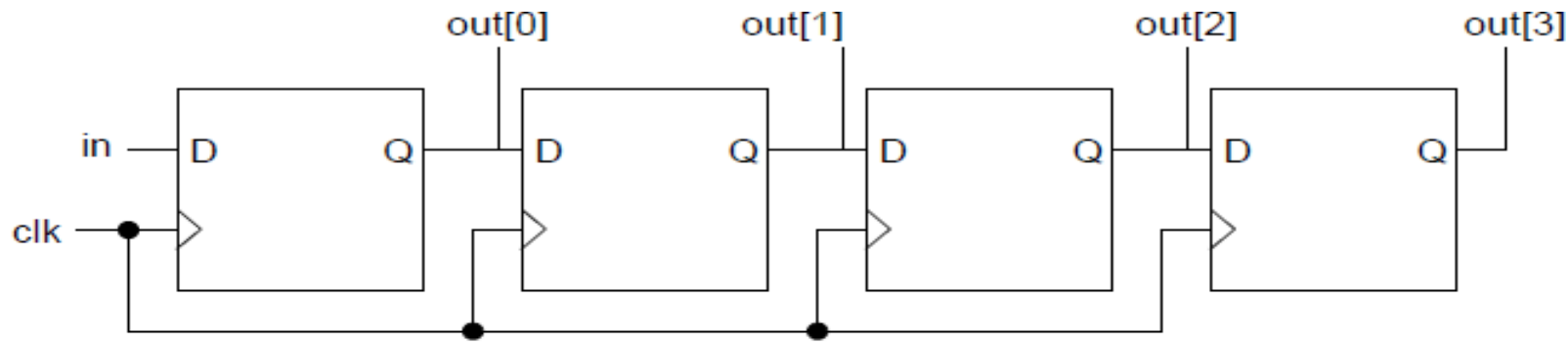
$\text{out} \leftarrow Q_2$

Input is 1-bit *in*, and output is 1-bit *out*

Serial In Parallel Out

- SIPO

- 4-bit SIPO shift register
 - 1-bit input *in*, and 4-bit output *out[3:0]*



when $\text{clk} = \uparrow$
 $\text{out}[0] \leftarrow \text{in},$
 $\text{out}[1] \leftarrow \text{out}[0]$
 $\text{out}[2] \leftarrow \text{out}[1]$
 $\text{out}[3] \leftarrow \text{out}[2]$

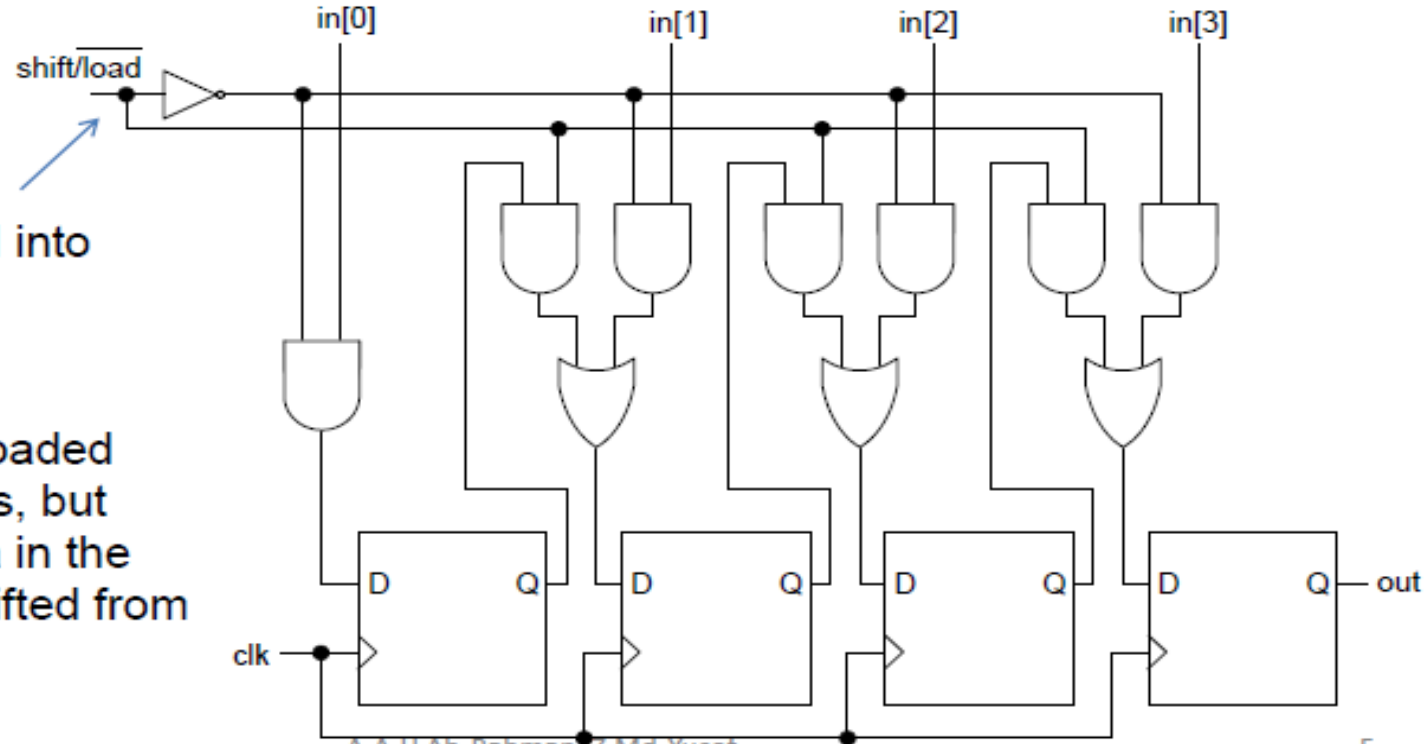
Parallel In Serial Out

– PISO

- 4-bit PISO shift register
 - 4-bit input $in[3:0]$ and 1-bit output out with sl

If $shift/load = 0$,
 $in[3:0]$ is loaded into
the flip-flops

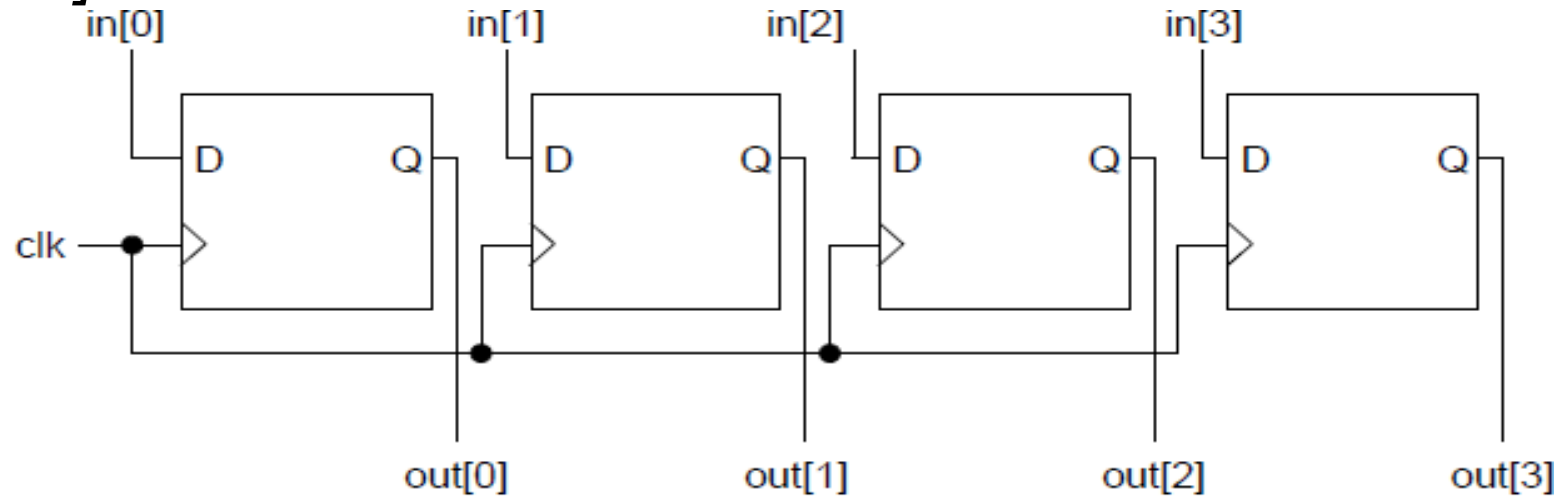
If $shift/load = 1$,
 $in[3:0]$ is NOT loaded
into the flip-flops, but
the current data in the
flip-flops are shifted from
left to right



Parallel In Parallel Out

– PIPO

- 4-bit PIPO shift register
 - 4-bit input $in[3:0]$ and 4-bit output $out[3:0]$



when $clk = \uparrow$
 $out[3:0] \leq in[3:0]$

End of
chapter VII